Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **Q2 (P) DRAIN**
2. **Q2 (P) SOURCE**
3. **Q2 GATES**
4. **Q2 (N) SOURCE**
5. **Q2 (N) DRAIN**
6. **Q1 GATES**
7. **VSS Q1, Q2, Q3 (N) SUBSTRATES, Q1 (N) SOURCE**
8. **Q1 (N) DRAIN**
9. **Q3 (N) SOURCE**
10. **Q3 GATES**
11. **Q3 (P) DRAIN**
12. **Q3 (N) DRAIN, Q3 (P) SOURCE**
13. **Q1 (P) SOURCE**
14. **VDD Q1, Q2, Q3 (P) SUBSTRATES, Q1 (P) DRAIN**

**1 14 13**

**2**

**3**

**4**

**5**

**6**

**7 8 9**

**12**

**11**

**10**

**MASK**

**REF**

**.042”**

**.047”**

**CD**

**4007**

**UBA**

**Top Material: Al**

**Backside Material: SiNi**

**Bond Pad Size: .0033” X .0033”**

**Backside Potential: FLOATING**

**Mask Ref: CD 4007 UBA**

**APPROVED BY: DK DIE SIZE .042” X .047” DATE: 2/16/17**

**MFG: TEXAS INSTRUMENTS THICKNESS .015” P/N: CD4007UB**

**DG 10.1.2**

#### Rev B, 7/1